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A comparative analysis on the Nanoscale of optimized FinFET transistors

Abdullah El-Bayoumi

Electronics and Electrical Communications Engineering Department, Cairo University, Giza, Egypt
Valeo InterBranch Automotive Software, Smart Village, Cairo-Alex Road, Giza, Egypt

Abstract

Fin-type Field-Effect Transistors (FinFETs) are the prospective promised solutions in deep submicron CMOS technologies due to the challenges that face MOSFET transistors, especially short-length channel. The short-channel transistor produces two current paths that control the channel barrier height due to the internal capacitances formation. The finFET is a double-gate transistor to improve the off-current and not to have a silicon far from the gate. In this paper, a comparative study on optimized finFET transistors alongside the nanoscale that enhances the short channel challenges is introduced. The finFET design enhancements include a silicon-on-insulator (SOI), shallow trench isolation (STI), Ultra-Thin Body SOI (UTBSOI), multi-gate structure and stacked-channel structure.

Keywords: FinFET; short-channel effects; shallow trench isolation; lithography; etching; silicon on insulator; STI; SOI.

1. Introduction

Gordon E. Moore, cofounder of Intel, has stated in his observation over the history of computer hardware that the number of transistors on integrated circuits doubles approximately every two years [1]. Such trend has kept on living until nowadays. The main factor governing this progress has been the reduction in transistor's minimum feature length. Scaling is the widely accepted terminology describing such a phenomenon due to reducing the circuit footprint. In other words, the process of reducing the minimum feature length of a transistor allows for more number of transistors on the same silicon area.

Transistors migration to deep submicron CMOS technologies, from the 0.5 µm technology downwards to smaller nodes and by going all the way down to 65 and 42 nm, leads to infamous phenomena [1]. In order to realize the drawbacks of short-length channel transistors [2], the performance of the long channel ones should be considered at first. Fig. 1 shows on the vertical axis the transistor's drain current in log scale and on the horizontal axis the gate voltage in volts. It's aimed to have the transistor characteristics to look like the bottom curve in red of Fig. 1. That is, the current is large when the transistor gate voltage (V_G) is high. In additions, if the gate voltage is reduced, the current should drop to a very low value which called off-current (I_{OFF}).

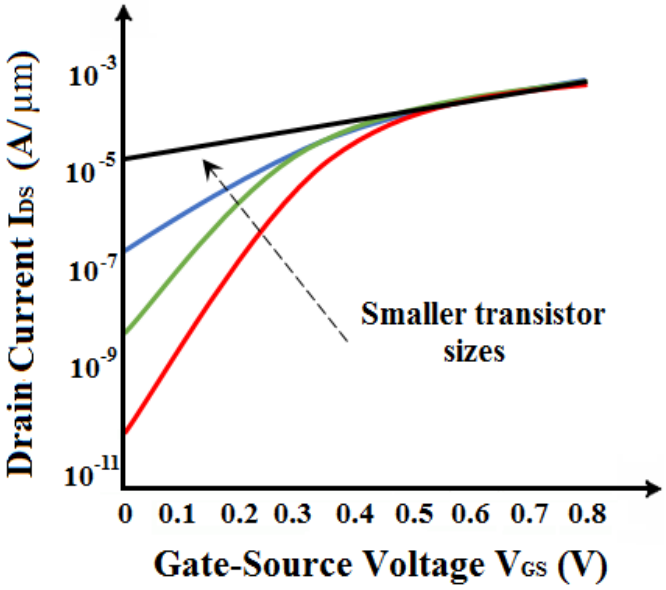

Fig. 1. Gate voltage versus drain current.

In the past 10 years in particular, the traditional planar MOSFET transistor looked more and more first like the green curve of Fig. 1. Meanwhile, it currently looks like the Fig. 1 blue curve. The slope of the curve near the off-region is called

Corresponding author: Abdullah El-Bayoumi
Email Id: abdullah.elbayoumi@yahoo.com

the sub-threshold swing. As the curve gets steeper, the transistor behaves better from the characteristics prospective.
It is preferable, at a certain sub-threshold swing, to increase the transistor threshold voltage in order to keep the off-current at a minimum value. This could be done by enlarging the supply voltage which results in producing more power consumption. Moreover, there is another main factor that increases the threshold which is the substrate doping. Regardless that high doping concentration leads to random variations inside a device due to revealing another degrading performance in what is known as mismatch [2].
Fig. 2 shows the cross section of a long channel transistor. The transistor gate controls the channel through the oxide capacitor (C_G). The dashed line, shown in Fig. 2, shows the potential barrier among the source gate, the drain gate and the formed channel between source and drain. It shows that between the source and the channel there's a potential barrier. This barrier resists electrons from moving from the source to the drain.

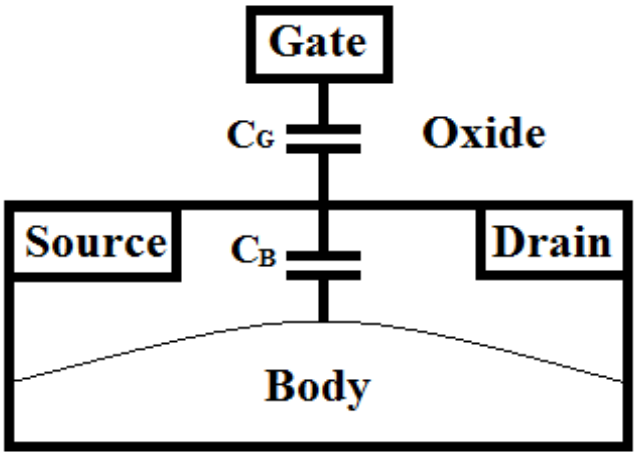

Fig. 2. Cross section of a long channel model

The height of the barrier is controlled by the transistor gate voltage which is stored in gate capacitances. With the help of that capacitance, the barrier height can be lowered in order to allow electrons to flow from the source through the channel into the drain. This either makes the transistor be in the on-state or raise the potential barrier height due to reducing the number of electrons that go through the channel and resemble the off-state. As the formed channel gets shorter, the process implies doping the channel more heavily. This provides a thin depletion layer. Consequently, a capacitance, which is formed between the channel and the body, tries to keep the barrier of the channel fixed by making it harder for the gate voltage to increase the barrier or lower it. Therefore the sub-threshold swing gets worse.
On the other hand, the short channel effect implies using a heavy channel doping to ignore the additional revealed capacitor shown between the drain and the original formed channel, as represented in Fig. 3 as C_D. This evolves two paths that control the channel barrier height [2]. The first path is formed between the drain and the gate with the help of C_G capacitor. While, the second path is formed between channel and the drain, as well, with the help of C_D capacitor. The drain to channel capacitances increase, once the distance between the source and drain gets shorted. So, if the channel is short enough, then there is no need to have any gate voltage once a voltage is applied on the drain (i.e. the channel turns on). Therefore, the current-voltage characteristic would be more like the topmost curve in Fig. 1.
This work focuses on discussing various designs of the finFET that could enhance MOSFET problems at deep submicron CMOS. The major MOSFET problems are the short-channel effect, drain-induced barrier lowering (DIBL), the off-current and the high consumed power. The extra dimension of the finFET shows a higher performance than the planar MOSFET structure.

2. Optimized FINFET Transistors

Device physics scientists has investigated dealing with short channel problems simply by making the transistor oxide much thinner [4]. This allows the transistor source and drain to get closer and closer. In additions, the boundaries of the oxide thickness might lead to figuring out the limit that should be between the drain and the source [3].

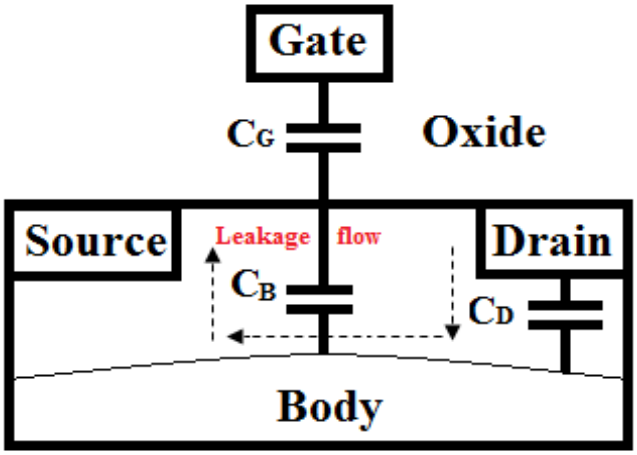

Fig. 3. Short channel Model.

The channel boundaries have been proved to be incorrect as illustrated in [4]. The reason is simple as the following example. If there is an invented ideal dielectric, it can be made as thick as few atomic layers. With a zero thickness, the gate capacitor (C_G) can be infinite. Even if this dielectric has no tunneling, no leakage and no reliability problems, the source and drain cannot be infinitely close. The reason is that ideal oxide will simply allow the gate to get a perfect control of the potential barrier along the oxide-semiconductor interface. Although, for potential leakage path that are as far as a few nanometers below that interface, are very far from the gate. In fact, they might be closer to the drain than to the gate. Hence, exhibiting a high K-dielectric does not allow to go any further. Another replacement of the MOSFET transistors' structure

should be maintained to face the short channel challenges by making no silicon or any sort of semiconductor. It is preferable to make the gate far from the semiconductor, because the gate is able to control it or even the silicon itself that is close to it. This solution has been introduced by the scientists from the University of California, Berkley [4], [5].

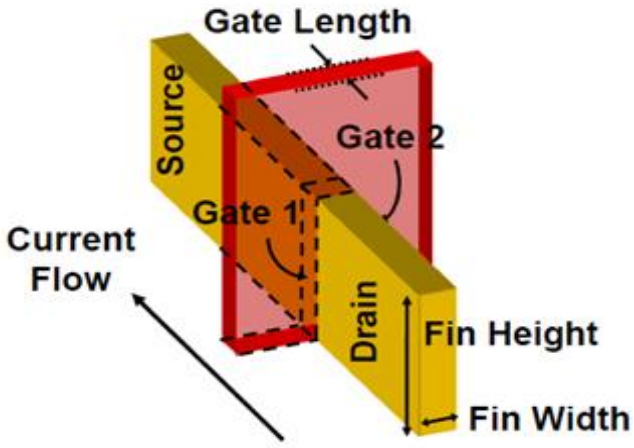

Fig. 4. finFET layout.

The reason behind the fin-type Field Effect Transistor (finFET) shape is to have such a simple structure to manufacture, as well as, not to have the silicon very far from the gate long (i.e. to be able to have shorter dimensional transistor) [6]. The finFET, as shown in Fig. 4, is a thin high-quality single crystalline sheet of silicon. It also has a self-aligned and connected 2 layers of dielectric placed on top and below, as well as, 2 layers of gate placed on top and below. The FINFET structure is rotated by 90 degrees to be easily implemented.

The horizontal source-body piece of the finFET is made by photolithography and etching. The whole finFET piece is considered the body of a transistor. The surface of the finFET is coated with a dielectric, and a gate is grown over the coating dielectric. The process of lithography and etching are done over and over to define the gate. After that, ion Implanting is done for the source and drain. This permits the current to flow along the 2 side surfaces along with the top surface of the finFET.

By the year 1997, The US Defense Advanced Research Projects Agency (DARPA) funded a project [5] where its results revealed at 1999. The results showed a 35 nm minimum feature length finFET utilizing a 30 nm thin fin with a sub-threshold swing of 66 *m*V/decade, a smaller leakage [7] of 10 $pA/\mu m$, and a reasonable current. The key to that was neither the shape nor the 3 dimensional structure gate. The key is that the fin itself is very thin. The thin fin was on a Silicon-on-Insulator (SOI) layer and was cut via an electron beam to be as thin as 30 nm. Consequently, the finFET idea is able to solve the scaling problems without needing any doping in the body or even any thinner dielectric.

Although, in the 2000's, finFET found its way as the likely successor to the planar transistor, it has such new scaling rules [6]. The simulations showed that this is not a generation invention. Likely scaling the gate length, the thin film thickness is also able to be scaled. In other words, silicon fins need to be only a little bit smaller than the gate length. As long as it's not larger than the gate length, short channel effects are suppressed.

In 2002, Advanced Micro Devices (AMD) showed a 10 nm finFET because they tried harder to make the film even thinner [8]. Meanwhile in 2004, Taiwan Semiconductor Manufacturing Company (TSMC) reached and published a 5 nm finFET [9]. Today, the record is held by the South Korean university KAIST (Korea Advanced Institute of Science and Technology), which has demonstrated a 3 nm finFET [10]. They illustrated that the only limit that restricts the transistor scaling is the limits of lithography.

Two major improvements have been proposed for the finFET. First, in 2002, TSMC stated that they had reached a good enough etch selectivity [9], whereas it is not necessary to keep an etch stop oxide above the fin. In other words, There is a thick oxide between the gate and the fin, because when etching the gate it is undesired for an over-etch to etch through the gate dielectric and eventually into the source and the drain portions of the fin. This is a mandatory step, as it gives the tri-gate transistor 2 gates on the sides and one at the top. Second, in 2003, SAMSUNG demonstrated that finFET could be made in a box of silicon instead of the 1999 finFET which was done on SOI due to the isolation easiness [11]. So, a Shallow Trench Isolation (STI) was utilized for on the bulk substrate.

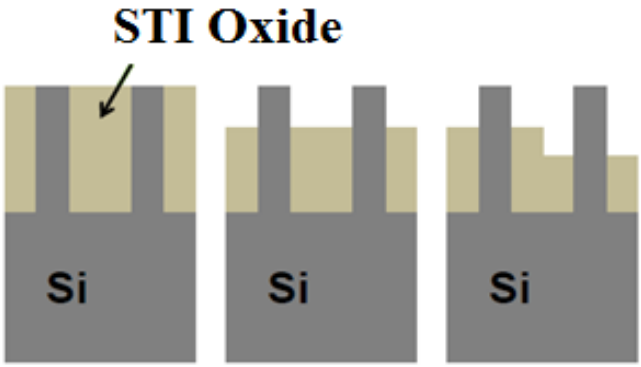

Fig. 5. FinFET using STI.

Growing a fin via STI, as shown in Fig. 5, is a quiet simple. Two closely-spaced shallow trenches should be created. So, lithography permits having a very thin film of silicon separating the trenches. After etching, both trenches leaves the very thin silicon film to be used as the body. Hence, multi-height fins could be generated by defining specific masks for etching and others to etch deeper into the oxide in order to make higher fins. Experimentally, STI is very compatible with the regular CMOS technology.

Intel has said that the cost difference in finFET technology and the planar transistors is 3 %. By the time, finFET becomes mainstream as this percentage may drop to 0% or even a negative percentage [5].

From the device footprint perspective, finFETs do not only reduce the minimum feature length of a transistor, but also their new architecture gives a new definition to the transistor's width [12]. Calculating a tri-gate finFET width would be adding both sides and the top gate. By assuming that body thickness is X nm and fin height is Y nm, the width equals to 2×Y+X. As a result, integer multiples of that width could be produced. By having only discrete width values, multiple fins could be. The main disadvantage is that varying the fin height changes the multiplier of the new width equation. For a simple industrial process and in order not to allow less control over transistor's effective width, the current finFET technologies provide only a fixed fin height.

An example to imagine this number of the saving transistor footprint is as the following with the fact that the fin width is smaller than the fin length. By assuming that it is a 20 nm technology with a fin width of 18 nm and a fin height of 30 nm, a single fin transistor width would be equal to 78 nm. This width is compared to the pitch of the fin which is being the horizontal space consumed by the finFET on a single chip. The corresponding fin pitch is about 45 nm. This results in a number of savings of 58 % in the footprint (45 nm instead of 78 nm).

A SPICE model has been produced by University of California, Berkeley (UCBK) to link the design community with the new technology. The model name is BSIM (Berkeley Short-channel Independent-Gate FET Model) [13]. The BSIM finFET model has been selected as the cost-free industry standard finFET model [14].

FinFET transistors provide a steeper turn off current, less variation than MOSFET and less footprint on the die of silicon. In additions, they solve short-channel effect problems. There is another technology developed by UCBK which is Ultra-Thin Body Silicon on Insulator (UTBSOI) which follows the same theorem as finFET in reducing the body thickness to reduce the far distance from gate effect. In UTBSOI, the challenge from the fabrication perspective is etching the silicon down to 3~4 nm [15]. Such a technology along with finFET and other transistor architecture resemble the gate to the scaling beyond the 15 nm borders.

3. Conclusion

In this paper various types of optimized finFET transistors are analyzed to solve the most commonly challenges of a planar MOSFET in deep submicron CMOS technology (i.e. short channel effects). Due to technology scaling, the transistor bulk requires an increase in doping level. This adversely affects the transistor carrier mobility and the junction capacitance. Hence, scaling to lower nodes such as 15-20 nm gate lengths is much difficult.

The finFET is originally developed for manufacture of self-aligned double-gate MOSFETs, so as to address the need for improved gate control to suppress I_{OFF}, drain-induced barrier lowering (DIBL) and process-induced variability for a transistor length less than 25 nm. Tri-Gate and bulk variations of the finFET have been developed to improve manufacturability and cost. The multi-gate MOSFETs provide a pathway to achieve lower power and/or improved performance. A further evolution of the MOSFET to a stacked-channel structure may occur by the end of the roadmap.

3.1 Advantages of finFET over the bulk

- It has reduced drain-source capacitances (oxide isolation versus junction isolation), and capacitances from substrate to metal interconnections. This provides a lower power dissipation.
- No MOSFET with the reverse body-effect exist in stacked transistor devices.
- It has an improved latch-up and noise and a current immunity through the substrate.
- It is a simpler high-voltage component design
- It has an improved high temperature performance due to lower device and parasitic leakage.
- It has improved passive components.
- It has a fewer process steps from the perspective of the pwell and the NBL.
- It provides a high-performance low-leakage low-power small-area system-on-chip.
- It adds an extra dimension (i.e. height) for an additional gate width.

3.2 Disadvantages of FinFET over Bulk

- It has self-heating and dissipation problems.
- It has a reduced supply-to-ground capacitance for noise reduction on supply rail
- It has larger start-up and substrate cost with extra design time compared to planar MOSFETs.
- Due to not maturity in a fixed enhancement, it has a limited knowledgebase.

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